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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.  | CONFIRMATION NO. |
|--|-------------|----------------------|----------------------|------------------|
| 10/766,465   | 01/27/2004  | Ling Ma              | IR-2444 CIP (2-3869) | 3194             |
| 2352   | 7590        | 11/22/2005           | EXAMINER             |                  |
| OSTROLENK FABER GERB & SOFFEN<br>1180 AVENUE OF THE AMERICAS<br>NEW YORK, NY 100368403 |             |                      | KIM, SU C            |                  |
|  |             |                      | ART UNIT             | PAPER NUMBER     |
|  |             |                      | 2823                 |                  |

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/766,465

Applicant(s)

MA ET AL.

Examiner

Su C. Kim

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 2 and 3 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 8/25/2004 & 1/06/2005
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

**REMARK / ARGUMENT**

By applicant' preliminary amendment on 01/06/2005, claims 2 & 3 are canceled.  
Now claims 1 & 4-10 are pending.

***Drawings***

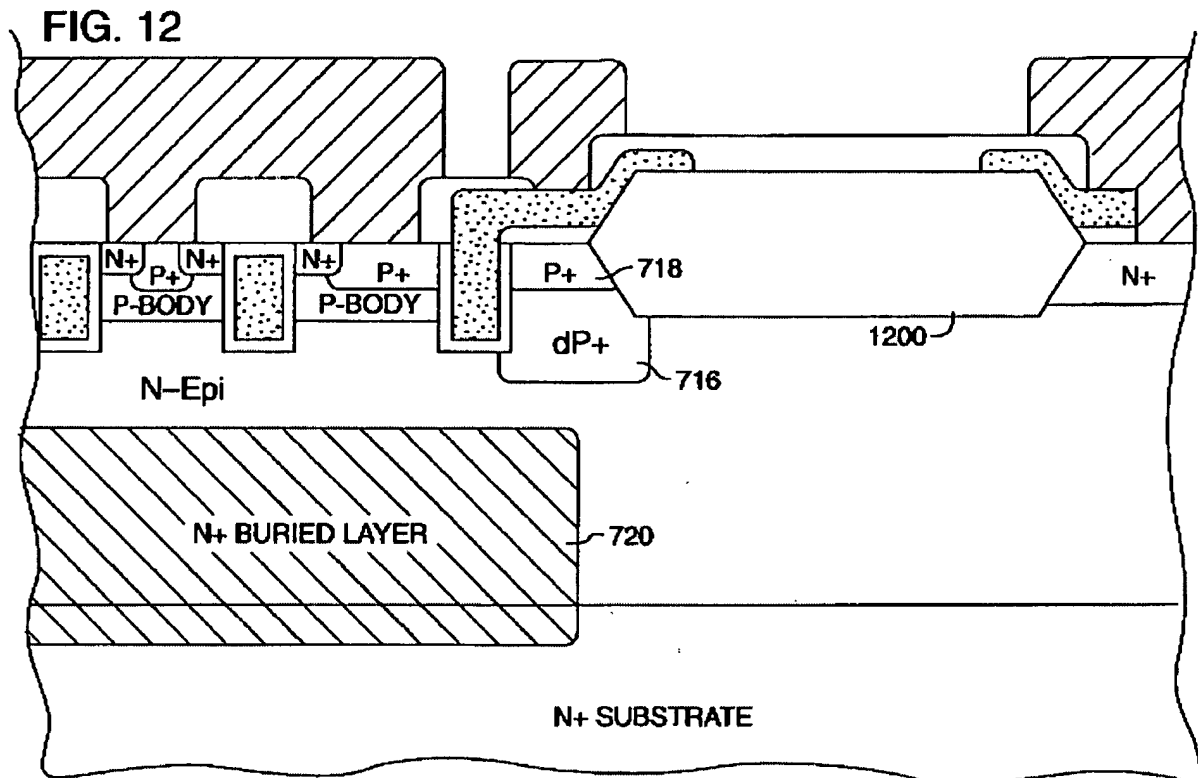
Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 7, & 8 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams (US 5814858) in view of Zeng (US Pub 2003/0205758).



Williams discloses DC-DC converter as claimed. **See all the FIGS** where Williams teaches the following limitations

1. Pertaining claim 1, Williams discloses a DC-DC converter comprising:

a synchronous semiconductor device; and

a control semiconductor device (**Please note Power MOSFET is synchronous semiconductor and control semiconductor device**) ;

wherein at least one of said semiconductor devices includes:

a semiconductor body of a first conductivity **708** which includes a channel region **708** of a second conductivity **706** and a major surface;

an active region (**Fig. 11**) formed in said semiconductor body, said active region including a trench **702** extending through said channel region and a gate structure **702** disposed in said trench which includes a gate oxide layer **1102** (Column 7 lines 29-30) disposed at least on said sidewalls of said trench and a gate electrode **702** disposed adjacent said a gate oxide layer: and

a termination structure(**Fig. 12**), said termination structure including, a termination trench formed in said semiconductor body, and a field oxide layer formed in said termination trench below said major surface (**Fig 12**),

Williams fails to teach a field oxide layer formed in said termination trench below said major surface is thicker than said gate oxide layer. Zeng discloses a field oxide layer formed in said termination trench below said major surface (**Fig. 15 please note the element 340 (Oxide layer) is thicker than the gate oxide layer 40**). In view of Zeng, it would have been obvious to one of ordinary skill in the art to incorporate the process step of Zeng into the Williams because "the power MOSFETs used in power management circuitry can be efficiently turned on and off at low gate drive voltage" (column 1 paragraph[0002] lines 8-10).

2. Pertaining claim 7, Williams in view of Zeng discloses a semiconductor device according to claim 1, wherein the depth of said trench has been selected to achieve an optimum figure of merit.

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodru* ; 919 f 2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizake*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

3. Pertaining claim 8, Williams in view of Zeng discloses a semiconductor device according to claim 1, wherein said trench is a stripe.

Claims 4- 6 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams (US 5814858) in view of Zeng (US Pub 2003/0205758) and further in view of Aoki et al. (US Pub 2002/0167046).

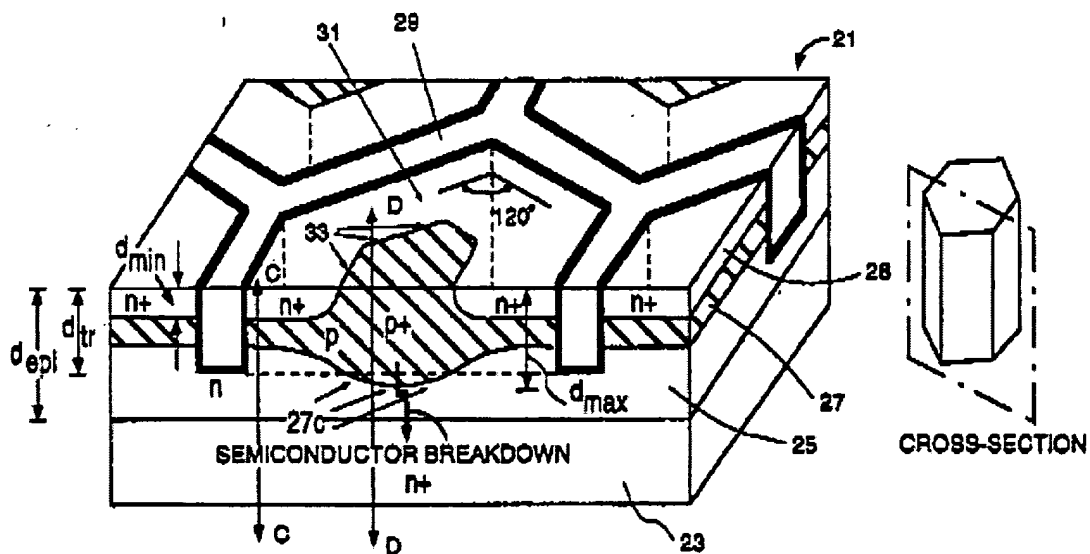
4. Pertaining claim 4, Williams in view of Zeng fails to teach trench including an oxide mass formed at its bottom said oxide mass being thicker than said gate oxide layer. Aoki discloses trench including an oxide mass formed at its bottom said oxide mass being thicker than said gate oxide layer (**Paragraph [0045] element 7e**). In view of Aoki, it would have been obvious to one of ordinary skill in the art to incorporate the trench of Aoki into Williams in view of Zeng because of "lower withstand voltage" (**paragraph [0005]**)

5. Pertaining claim 5, Williams in view of Zeng discloses a semiconductor device according to claim 4, wherein said semiconductor body includes conductive regions **706** of said first conductivity formed adjacent said trench in said channel region **708**, and further comprising a semiconductor substrate of said conductivity **714**, said semiconductor body being formed over said semiconductor substrate, wherein said conductive regions are electrically connectable to said semiconductor substrate through invertible channels adjacent said trench (**Fig. 11H, Please note the power MOSFET**

has conductive regions 706, which are electrically connectable to semiconductor substrate through invertible channels).

6. Pertaining claim 6, Williams in view of Zeng discloses a semiconductor device according to claim 5, wherein said conductive regions are source regions **706**.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being anticipated by Williams (US 5814858) in view of Zeng (US Pub 2003/0205758) and further in view of Bulucea et al. (US 5298442)



Bulucea discloses a semiconductor device as claimed. **See all the FIGS** where Bulucea teaches the following limitations



7. Pertaining claim 9, Williams in view of Zeng fails to teach a semiconductor device according to claim 1, wherein said trench is a cell. Bulucea discloses a semiconductor device according to claim 1, wherein said trench is a cell (**Fig. 8**). In view of Bulucea, it would have been obvious to one of ordinary skill in the art to incorporate the process step of Bulucea into the Williams in view of Zeng because "maximizes the gate dielectric breakdown voltage and also provides position of voltage breakdown initiation to allow use of controlled bulk semiconductor breakdown." (**Column 1 lines 59-61**)

8. Pertaining claim 10, Williams in view of Zeng fails to teach a semiconductor device according to claim 9, wherein said cell is hexagonal. Bulucea discloses the cell is hexagonal. (**Fig. 8**)

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Su C. Kim  
11/16/2005

A handwritten signature in black ink, appearing to read 'W. David Coleman', with a large, sweeping loop at the end.

**W. DAVID COLEMAN  
PRIMARY EXAMINER**